Virtus Academy Course Prerequisite Map

1,551 words · ~7 min read

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*VCA cross-course quick-reference handout. Anchors: `website/index.html` catalog + the 12 course pages' Prereq sections + 5 (Part-II elective ordering). *

Purpose: unified course prerequisite map across all 12 currently-shipped Virtus Academy courses, with recommended track sequences for student onboarding and advisor reference. Print and pin in the lab or use for advising. **Use cases:** cohort orientation, transfer-credit-equivalency conversations, "what should I take next?" advising, dependency planning across multi-term enrollment.

At a glance

Property	Value
Courses currently shipped	12 (5 belt-1/2 entry + 4 belt-3/4 intermediate + 3 belt-4/5 capstone)
Recommended belt-ladder	5 dots: `1` (entry) → `5` (capstone)
Track sequences	5 named tracks (Foundations / Pentest / RE / Console / Adversarial)
Concurrent-eligibility	Most belt-1/2 courses can run concurrently
Capstone bottleneck	RE-101 + ADV-101 require multi-prereq convergence
Future expansions	CSA-201, con-101, AI-101/201/301, Adv-102 LLM-CVE variant. Placement noted at end

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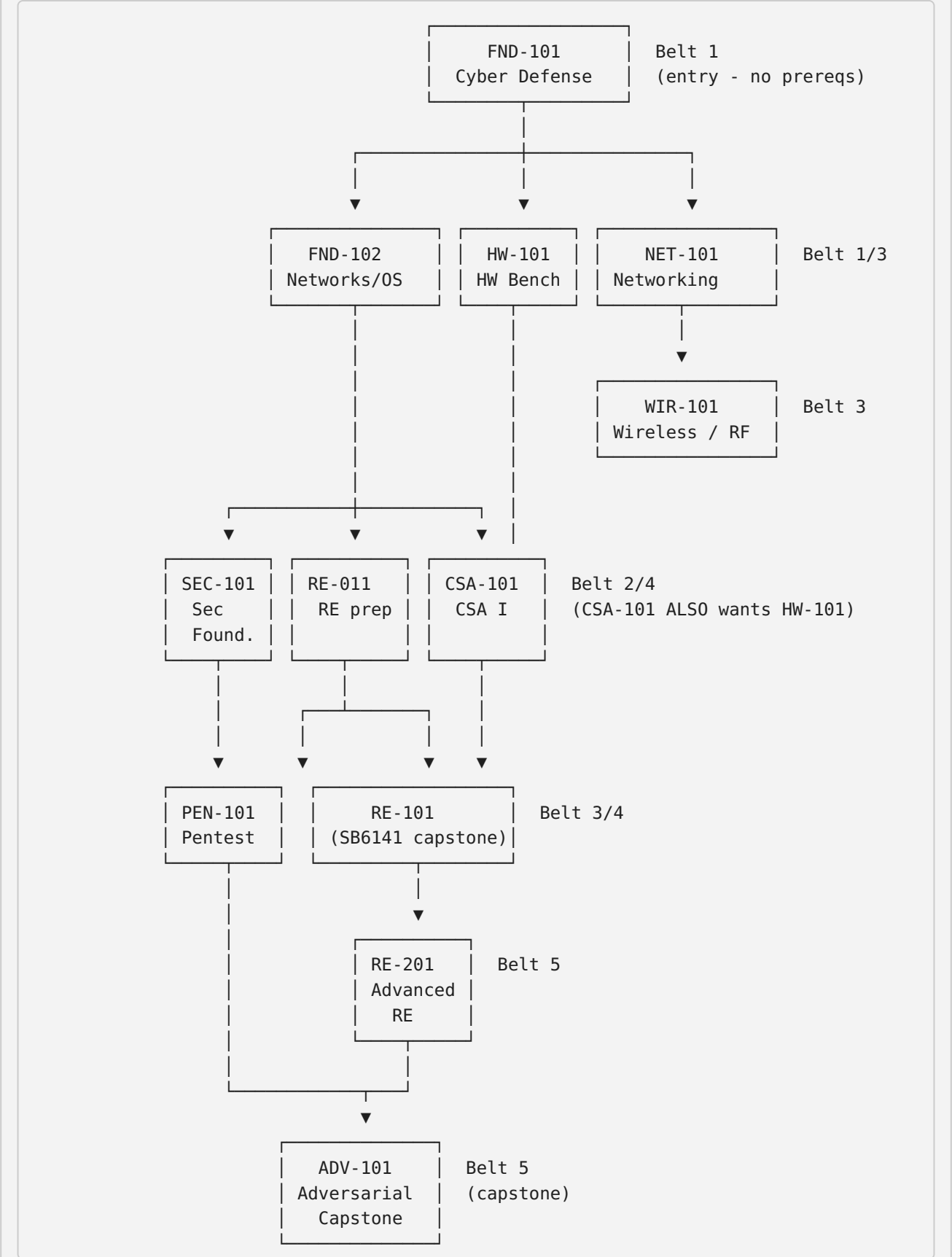
The 12 currently-shipped courses

Code	Title	Belt	Format	Lab home
FND-101	Foundations of Cyber Defense	1	online + lab	laptop
FND-102	Foundations II: Networks & Operating Systems	1	online + lab	laptop
HW-101	Hardware Lab Bench	3	hands-on	breadboard + multimeter + jumper kit
NET-101	Networking Fundamentals	3	online + lab	laptop + virtual networking
WIR-101	Wireless & RF Security	3	hands-on	wireless adapters + SDR (optional)
SEC-101	Cybersecurity Foundations	2	online	laptop
RE-011	Reverse Engineering Pre-Flagship Scaffolding	2	online + lab	laptop (Ghidra + radare2)
PEN-101	Pentest 101	3	online + lab	laptop + Kali
CSA-101	Computer Systems Architecture I	4	hands-on (heaviest hardware course)	Tang Primer 25K (canonical student target; Tang Nano 20K supported as advanced-track alternative) + HDMI monitor + DS2 controller (PMOD_DS2x2)
RE-101	Reverse Engineering (with SB6141 lab target)	4	hands-on	laptop + SB6141 + USB-TTL serial
RE-201	Advanced Reverse Engineering	5	hands-on	RE-101 setup + advanced fixtures
ADV-101	Adversarial Capstone	5	hands-on	full prior-track tooling

The map (visual)


FND-101
Cyber Defense
Belt 1
(entry - no prereqs)
FND-102
Networks/OS
HW-101
HW Bench
NET-101
Networking
Belt 1/3
WIR-101
Wireless / RF
Belt 3
SEC-101
Sec
Found.
RE-011
RE prep
CSA-101
CSA I
Belt 2/4
(CSA-101 ALSO wants HW-101)
PEN-101
Pentest
RE-101
(SB6141 capstone)
Belt 3/4
RE-201
Advanced
RE
Belt 5
ADV-101
Adversarial
Capstone
Belt 5
(capstone)

Edge list (machine-readable for advisor scripts)

```
FND-101 → FND-102
FND-101 → HW-101            (HW-101 also OK concurrent with FND-101)
FND-101 → NET-101

FND-102 → SEC-101
FND-102 → RE-011
FND-102 → CSA-101           (CSA-101 also requires HW-101)

HW-101  → CSA-101
NET-101 → WIR-101
NET-101 → PEN-101           (NET-101 strongly recommended; not strict prereq)

SEC-101 → PEN-101
SEC-101 → RE-101            (combined with CSA-101 + RE-011)

RE-011  → RE-101
CSA-101 → RE-101
RE-101  → RE-201

PEN-101 → ADV-101
RE-101  → ADV-101
RE-201  → ADV-101           (recommended; not strict)
```

Read these as `prereq → unlocks`. A course can be entered once *all* its incoming edges are satisfied.

Prereq table (per-course)

For each course: full prereq list + concurrent-eligible peers + suggested follow-on courses.

Course	Prereqs (must complete first)	Concurrent OK with	Recommended follow-ons
FND-101	(none)	(none)	FND-102, HW-101, NET-101
FND-102	FND-101	HW-101, NET-101	SEC-101, RE-011, CSA-101
HW-101	FND-101	FND-102, NET-101	CSA-101 (central prereq)
NET-101	FND-101	FND-102, HW-101	WIR-101, PEN-101
WIR-101	NET-101	SEC-101, RE-011	PEN-101, ADV-101
SEC-101	FND-102	RE-011, NET-101	PEN-101, RE-101
RE-011	FND-102	SEC-101, CSA-101 (early)	RE-101, RE-201
PEN-101	SEC-101 (NET-101 strongly recommended)	RE-011	ADV-101
CSA-101	FND-102 + HW-101	RE-011	RE-101, *future* CSA-201, *future* con-101
RE-101	CSA-101 + RE-011 + SEC-101	(concurrent CSA-101 is OK if RE-011 is done)	RE-201, ADV-101
RE-201	RE-101	(none. Capstone-class)	ADV-101
ADV-101	PEN-101 + RE-101 (RE-201 recommended)	(none. Capstone)	(graduate of curriculum)

Key: "concurrent OK" means the cohort-management software permits enrollment in both simultaneously; pedagogically, the courses interleave well (no dependent material across the pair). "Recommended follow-on" means the course's lab work and exit projects naturally lead into the listed targets.

Recommended track sequences

Five named tracks, each a coherent sequence of 4-6 courses telling one story about the discipline. Students can mix tracks; advisors recommend committing to one as a *primary* track for scheduling discipline.

Track 1. Foundations Track (general practitioner literacy)

```
FND-101  →  FND-102  →  SEC-101  →  NET-101  →  PEN-101
```

- **Audience**: general cybersecurity practitioner; transfer student from a non-cyber CS program; defensive-side career path.
- **Total commitment**: 5 courses; ~14-18 cohort-weeks if sequential.
- **Exit competency**: can perform routine security analysis, network defense, basic pentesting.
- **Belt earned**: 1 → 3.

Track 2. Pentest Track (offensive operator path)

```
FND-101  →  FND-102  →  SEC-101  →  NET-101  →  WIR-101  →  PEN-101  →  ADV-101
```

- **Audience**: red-team / pentest career path; offensive-security focus.
- **Total commitment**: 7 courses; ~20-24 cohort-weeks if sequential.
- **Exit competency**: full-stack pentest engagement; wireless attack chain; adversarial mindset against arbitrary networked systems.
- **Belt earned**: 1 → 5.

Track 3. Reverse Engineering Track (RE path)

```
FND-101  →  FND-102  →  SEC-101  →  RE-011  →  CSA-101  →  RE-101  →  RE-201
```

- **Audience**: firmware-RE ; vulnerability-research career path; CTF binary-analysis competitor.

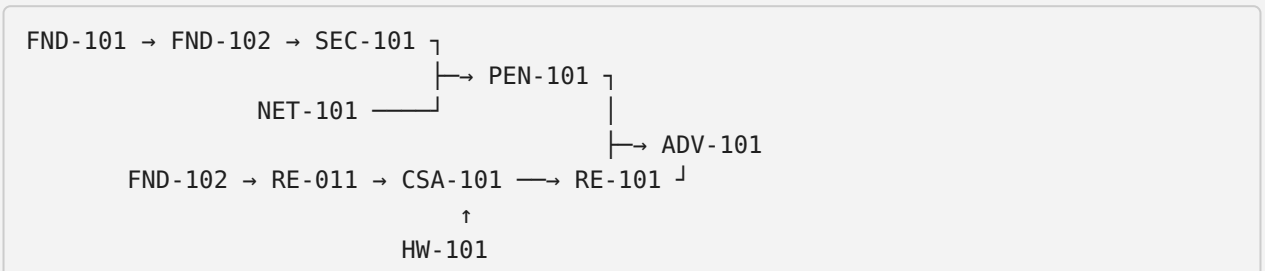
- **Total commitment**: 7 courses; ~24-32 cohort-weeks (CSA-101 is a 14-week heavy course; RE-101 is 12-week).
- **Exit competency**: dissect arbitrary firmware binaries (ARM / RISC-V / x86); decompile + reverse OS-level structures; capstone-class SB6141 firmware understanding.
- **Belt earned**: 1 → 5.

Track 4. Console / Deep-CS Track (the curriculum's hardest track)

```
FND-101  →  FND-102  →  HW-101  →  CSA-101  →  *future* con-101  →  *future*
CSA-201
```

- **Audience**: hardware-security ; embedded firmware engineer; FPGA + low-level systems career path.
- **Total commitment**: 4 currently-shipped + 2 future = 6 courses; ~30 cohort-weeks (CSA-101 alone is 14 weeks; CSA-201 likely 14-16).
- **Exit competency**: builds working CPUs on FPGAs; writes complete OS from scratch; understands every byte from gate to GUI; **owns every layer of the apparatus**.
- **Belt earned**: 1 → 5 (con-101 is currently belt-4; CSA-201 will be belt-5).

Track 5. Adversarial Track (the most-prereqs-heavy track)



- **Audience**: full-stack adversary; nation-state-class operator path; advanced red team.

- **Total commitment**: 9 courses; ~40+ cohort-weeks (the curriculum's most demanding track by total contact hours).
- **Exit competency**: complete adversarial capability across networked, hardware, firmware, and human-target attack surfaces.
- **Belt earned**: 1 → 5.

Concurrent-enrollment matrix

Which courses can a student take *at the same time* without pedagogical conflict?

	FND-101	FND-102	HW-101	NET-101	WIR-101	SEC-101	RE-011	PEN-101	CSA-1
FND-101	-	(prereq)	✓	✓	(no)	(no)	(no)	(no)	(no)
FND-102	(prereq)	-	✓	✓	(no)	(no)	(no)	(no)	(no)
HW-101	✓	✓	-	✓	(no)	(no)	(no)	(no)	✓*
NET-101	✓	✓	✓	-	(prereq)	✓	✓	✓	(no)
WIR-101	(no)	(no)	(no)	(prereq)	-	✓	✓	✓	(no)
SEC-101	(no)	(no)	(no)	✓	✓	-	✓	(prereq)	(no)
RE-011	(no)	(no)	(no)	✓	✓	✓	-	✓	✓*
PEN-101	(no)	(no)	(no)	✓	✓	(prereq)	✓	-	(no)
CSA-101	(no)	(no)	✓*	(no)	(no)	(no)	✓*	(no)	-
RE-101	(no)	(no)	(no)	(no)	(no)	(prereq)	(prereq)	(no)	(prerec
RE-201	(no)	(no)	(no)	(no)	(no)	(no)	(no)	(no)	(no)
ADV-101	(no)	(no)	(no)	(no)	(no)	(no)	(no)	(prereq)	(no)

Legend:

- ✓ = concurrent enrollment allowed
- ✓* = concurrent allowed but pedagogically tight; advisor counsel recommended
- **(prereq)** = the row course is a prereq for the column course (or vice versa)
- **(no)** = pedagogical conflict; sequential enrollment recommended

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Belt ladder (5 dots from entry to capstone)

Belt	Earned by completing	Concretely means
1	FND-101	Cohort orientation complete; basic cyber literacy
2	FND-102 + SEC-101	Practitioner-grade defensive vocabulary; OS & networking fundamentals
3	NET-101 + WIR-101 + PEN-101 + HW-101 + RE-011 (any 2 of the 5)	Specialist-track entry; production tooling literacy
4	CSA-101 + RE-101 (one or both)	Capstone-class artifact ownership; SB6141 firmware-reading capability
5	RE-201 + ADV-101	Adversarial mastery; original-research capability

The 5-dot belt-ladder displays on every Virtus Academy course page (top-right header in the rendered website).

Future expansions (placement notes)

The currently-shipped 12 are the curriculum's *spine*. Expected expansions land in known places on the map:

Course	Expected belt	Prereqs	Slot
CSA-201	5	CSA-101	Console-Track-4 follow-on; extends RV32I-Lite to full RV32I + M extension; adds privilege boundary + MMU
con-101	4	CSA-101	"Virtus Console: Retro Cores & Homebrew". Deep-FPGA console-programming course; sequence parallel to RE-101
AI-101	2	FND-102	AI/agentic-system security entry; sits parallel to SEC-101 in Foundations Track
AI-201	4	AI-101 + SEC-101	Mid-tier AI-security; production-grade prompt-injection / model-extraction work
AI-301	5	AI-201 + RE-101	Capstone AI-security; agentic-system adversarial research
Adv-102 (LLM-CVE variant)	5	ADV-101 + AI-201	LLM-specific adversarial deep-dive; references CVE-2025-65106 (LangChain Jinja2) and successors

The map is intentionally extensible. *Each new course slots into the existing sequence by inheriting one or two prereqs; the belt-ladder accommodates new courses by widening at the appropriate level.*

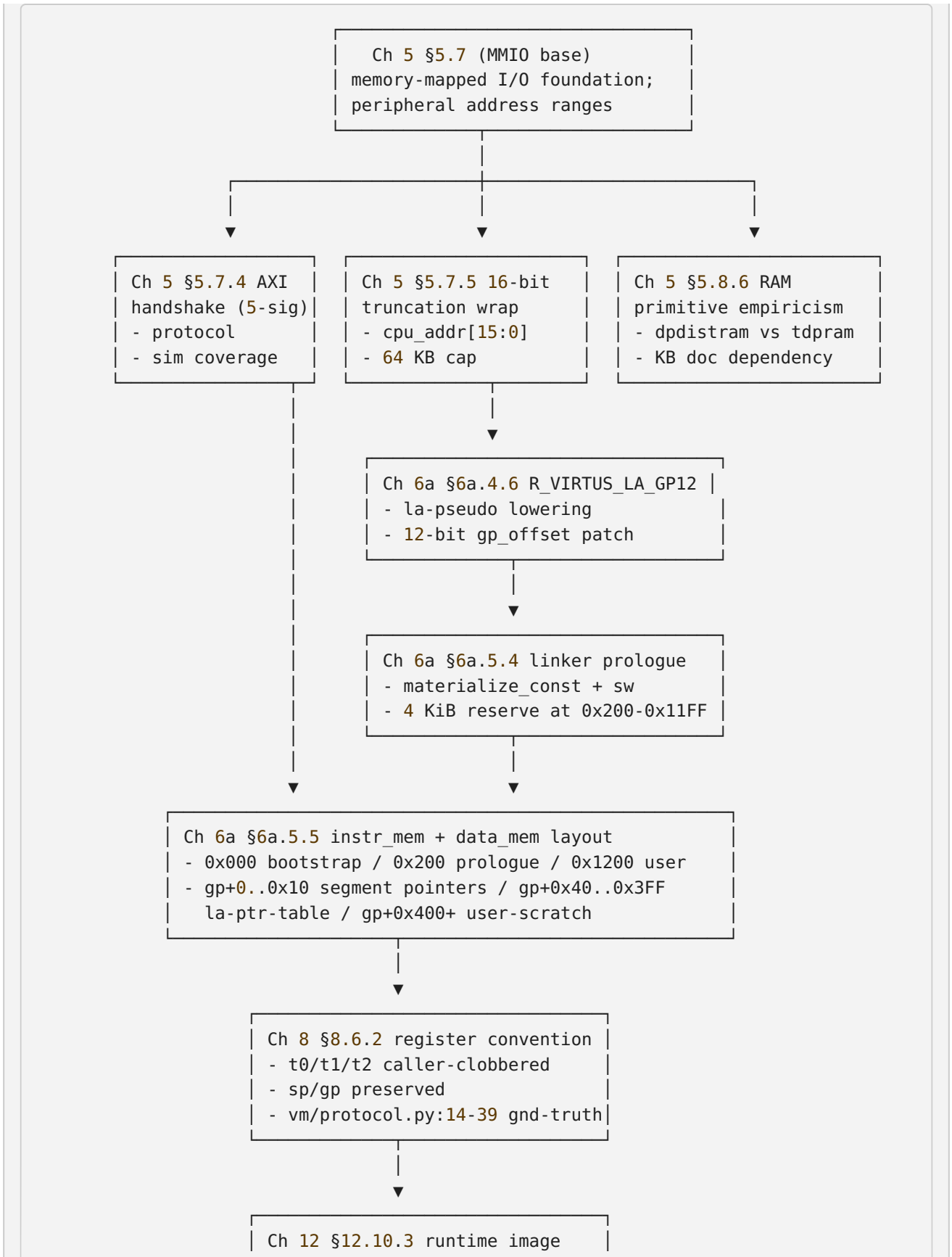
Advisor cheat-sheet

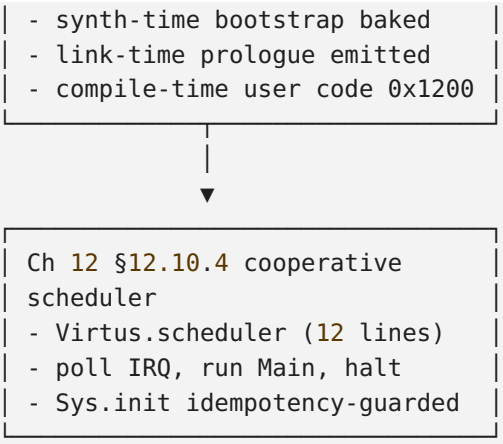
For "I'm a student who wants to do X, what should I take?":

Goal	Recommended sequence
"I want to do basic cyber defense"	Foundations Track
"I want to do red team / pentest"	Pentest Track
"I want to do firmware reverse engineering"	RE Track
"I want to build hardware / FPGAs / OS-level systems"	Console / Deep-CS Track
"I want to do nation-state-class adversarial work"	Adversarial Track
"I want to specialize in AI security"	Foundations Track + (future) AI-101/201/301 sub-track
"I want to do CTF binary-analysis competitions"	RE Track + ADV-101
"I want to be a hardware security researcher"	Console / Deep-CS Track + RE-201
"I'm interested in firmware vulnerability research"	RE Track + Adv-102 (LLM-CVE variant when shipped)

CSA-101 internal-runtime dependency chain

The cross-course prerequisite map above operates at course-level granularity. Inside CSA-101, the later chapters reveal a dependency chain that students need to navigate. This sub-poster documents that intra-course dependency chain so students can plan their reading order and understand which chapter contributes which piece of the runtime-image substrate.


Ch 5 §5.7 (MMIO base)
memory-mapped I/O foundation;
peripheral address ranges
Ch 5 §5.7.4 AXI handshake (5-sig)
- protocol
- sim coverage
Ch 5 §5.7.5 16-bit truncation wrap
- cpu_addr[15:0]
- 64 KB cap
Ch 5 §5.8.6 RAM primitive empiricism
- dpdistram vs tdpram
- KB doc dependency
Ch 6a §6a.4.6 R_VIRTUS_LA_GP12
- la-pseudo lowering
- 12-bit gp_offset patch
Ch 6a §6a.5.4 linker prologue
- materialize_const + sw
- 4 KiB reserve at 0x200-0x11FF
Ch 6a §6a.5.5 instr_mem + data_mem layout
- 0x000 bootstrap / 0x200 prologue / 0x1200 user
- gp+0..0x10 segment pointers / gp+0x40..0x3FF
la-ptr-table / gp+0x400+ user-scratch
Ch 8 §8.6.2 register convention
- t0/t1/t2 caller-clobbered
- sp/gp preserved
- vm/protocol.py:14-39 gnd-truth
Ch 12 §12.10.3 runtime image



Reading order (recommended): Ch 5 §5.7 + §5.7.4 + §5.7.5 (MMIO foundation + handshake protocol + truncation wrap) → Ch 5 §5.8 + §5.8.6 (synthesis + RAM primitive empiricism) → Ch 6a §6a.4.6 (la-pseudo) → Ch 6a §6a.5.4 + §6a.5.5 (linker prologue + memory layout) → Ch 8 §8.6.2 (register convention) → Ch 12 §12.3.2 (syscall dispatcher) → Ch 12 §12.10.3 + §12.10.4 (runtime image + scheduler).

Cross-chapter handouts that distill this chain: `cross-chapter-rv32i-lite-encoding-card.md` (register convention + ISA), `cross-chapter-vm-segment-cheat-sheet.md` (calling-convention diagram + saved-frame layout), `cross-chapter-instr-mem-layout.md` (instruction and data memory partition).

The chain represents the careful spec of the runtime image; CSA-101 chapter prose documents the dependencies in the order shown here.

Where to read more

- **`website/index.html`**. Public catalog with live belt-ladders + Equipment rows + Course Overviews per course.
- **Per-course pages** (`website/vca-{code}.html`), Prerequisites section on each.
- **Per-course pages** (`website/vca-{code}.html`), course overviews and equipment rows per course.
- **`PROJECT.md`** / **`README.md`**. Academy mission + 5-track-design rationale.
- **`Equipment`** **row on each course page**, what physical materials the course needs.

- **Silicon-level reading guides** (forward-reading after Ch 5): once you complete CSA-101 Ch 5 and ship your first FPGA bitstream, `cross-chapter-silicon-level-reading-guide.md` and `cross-chapter-fpga-cell-to-silicon-bridge.md` show you what the abstractions you just implemented look like in fabricated silicon. The reading guide walks through the MOS 6502 and Z80 using open-license interactive die-shot tools; the bridge handout connects your synthesized LUT4 cells and flip-flops to their physical silicon equivalents on the Tang Primer 25K. Neither is required reading before Ch 6, but students who want to see the physical layer beneath the Verilog abstraction will find both worthwhile.
